Remarks

Claims 1-110 are pending in this application and have been rejected by the Examiner under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. patent publication number 2003/0108195 to Okada et al. ("Okada et al."). No Claims are amended with this response. No new matter is added. Reconsideration and withdraw the outstanding rejections in light of the remarks that follow is respectfully requested.

Okada et al. is Not Prior Art under 35 U.S.C. § 102(e)

Okada et al. was filed after the invention by Applicant in the present patent application, and is therefore not prior art under 35 U.S.C. § 102(e).

In particular, Applicant respectfully points out that the Declaration filed with the present application on January 4, 2002 was in fact executed by the inventor on October 1, 2001. A copy of the Declaration as filed is attached hereto. The filing date of Okada et al. is January 3, 2002. Thus, the invention by Applicant occurred at least three months before the filing of the Okada et al. application. Okada et al. is therefore not available as a prior art reference under 35 U.S.C. § 102(e). Accordingly, withdrawal of the rejections of claims 1-110 under 35 U.S.C. § 102(e) is respectfully requested.

Applicants also note that the Filing Date listed on the Office Action Mailed December 13, 2005 bears an incorrect date of 04/15/2002. The correct Filing Date is January 4, 2002, as evidenced by the attached official Filing Receipt.

Claims 1-110 are patentable over Okada et al.

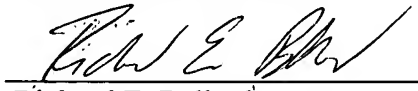
Applicant respectfully asserts that, even if Okada et al. was available as prior art under 35 U.S.C. § 102(e), none of Applicant's claims 1-110 would be anticipated by Okada et al. In particular, Okada does not teach or suggest any encryption/decryption circuit or method utilizing a staged pipeline logic circuit as described and claimed by Applicant, e.g., see FIGS. 15-21 (multiplication and division circuits) and FIGS. 40-45 (key expansion circuits). In contrast, Okada et

al. discloses a fundamentally different limited logic iterative approach where a processing algorithm is heavily repeated. The staged pipeline logic circuits of the present invention utilize replicated hardware for processing at each stage, which allow for much higher processing speeds than the iterative algorithm approach of Okada. Thus, Okada does not teach each and every limitation of any of Applicants claims 1-110.

For at least the reasons above, claims 1-110 would not be anticipated by Okada et al. Accordingly, withdrawal of the rejection of claims 1-110 is respectfully requested.

It is not believed that any fees are required beyond those that are provided for in the accompanying Petition for Extension of Time.

Respectfully submitted,

Date: June 13, 2006  46,078

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Enclosures:

Declaration of Darryl J. Van Buer, dated October 1, 2001
Official Filing Receipt
Petition for Extension of Time (3 Months)